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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

TC 2800 MAIL ROOM

In re Application of

Shrivastava

Serial No. 09/315,599

Filed: 05/20/99

For: **METHOD AND APPARATUS
FOR INTEGRATING FLASH
EEPROM AND SRAM CELLS
ON A COMMON SUBSTRATE**

Group Art Unit: 2814

Examiner: Ha, N.

**RESPONSE TO FINAL OFFICE
ACTION MAILED ON Sept. 26, 2001**

260 Sheridan Ave., Suite 420
Palo Alto, CA 94306
(650) 833-0160

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

REMARKS

Applicants respectfully request further examination and reconsideration in view of the comments set forth fully below. Within the Office Action, all of the Claims 1-10 were rejected. Claims 1-10 still remain pending.

Rejections Under 35 U.S.C. § 103

Claims 1-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,605,853 to Yoo et al. (hereinafter "Yoo") in view of U.S. Patent No. 5,679,599 to Mehta (hereinafter "Mehta"). The Applicant respectfully disagrees with this rejection.

Yoo teaches a method of forming a SRAM, a floating gate memory, and a logic device on the same integrated circuit. Specifically, Yoo teaches a method of forming simultaneously a SRAM and an EEPROM on the same integrated circuit, using a LOCOS isolation process. [Yoo, col 3, lines 51-55] Yoo teaches a method of forming a plurality of field isolation regions using a LOCOS isolation process. [Yoo, col 3, line 55-60] Yoo does not teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a non-LOCOS isolation process, such as a shallow trench isolation (STI) process. Nor does Yoo teach or suggest that a SRAM and an

EEPROM can be formed on the same IC, using a combination of a LOCOS and STI isolation process.

Mehta teaches a device and method for isolating regions of the circuit device in a semiconductor substrate. The method comprises the following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. [Mehta, Abstract and col. 4, line 46- col. 6, line 49] Mehta teaches a method of combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *simultaneously* forms a portion of the LOCOS region and trench isolation structure. [Mehta, col 4, line 47-51] However, Mehta does not teach or suggest combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *independently* or *sequentially* forms a portion of the LOCOS region and trench isolation structure. Furthermore, Mehta does not teach a separation technique for growing flash EPROM and SRAM on a common substrate.

As discussed above, Yoo does not teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a non-LOCOS isolation process, such as a shallow trench isolation (STI) process. Nor does Yoo teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a combination of a LOCOS and STI isolation process. Also, as discussed above, Mehta does not teach or suggest combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *independently* or *sequentially* forms a portion of the LOCOS region and trench isolation region. Nor does Mehta teach a separation technique for growing flash EPROM and SRAM on a common substrate. Accordingly, neither Yoo, Mehta nor their combination teach or suggest a system for independently or sequentially integrating SRAM cells and flash EPROM cells onto a single silicon substrate. Further, neither Yoo, Mehta nor their combination teach or suggest forming a SRAM and an EEPROM on a single substrate using a combination of a LOCOS and STI isolation process.

Within the Office Action, in the Response to Arguments section, it is concluded that the combination of Yoo and Mehta teaches the technique of using LOCOS and STI isolation techniques on an SRAM and EEPROM on the same substrate. The Applicant respectfully disagrees with this conclusion. A *prima facie* case of obviousness has not been met based on the

teachings of Yoo and Mehta. To establish a *prima facie* case of obviousness, three basic criteria must be met. There must first be some suggestion or motivation demonstrated, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of the references. Secondly, there must be a demonstration that the combination of the prior art references would result in a reasonable expectation of success. Finally, the combination of the prior art references must teach or suggest all the claim limitations. [M.P.E.P § 2142 - 43.]

There is no suggestion or motivation to combine Yoo and Mehta. As discussed above, Yoo teaches away from including a SRAM and an EEPROM on the same IC, isolated by a combination of a LOCOS and a second isolation technique. Furthermore, Mehta does not teach or otherwise indicate that the first and second isolation technique can be applied to isolate a SRAM and a EEPROM on a common IC. Therefore, it would not have been obvious to one skilled in the art to combine the teachings of Yoo and Mehta. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In Re Mills*, 916 F.2d 680, 16 USPQ2d 1420 (Fed. Cir. 1990). Within the current Office Action, there has not been any reference to any teaching, hint or suggestion in either Yoo and Mehta suggesting the desirability of a combination of these two references.

Further, there is no indication in the prior art that a combination of Yoo and Mehta would result in a reasonable expectation of success. As indicated by Yoo, in column 2, lines 18-26, a combination of a SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* [Yoo, column 2, lines 23-26] Furthermore, the teachings of Mehta do not indicate or suggest that the first and second isolation technique can be applied to isolate a SRAM and an EEPROM on a common IC. The combination of the teachings of Yoo and Mehta would not have resulted in a reasonable expectation of success. Therefore, the combination of the teachings of Yoo and Mehta does not render the current invention obvious.

In contrast to the teachings of Mehta, Yoo and their combination, the present invention teaches a system for *independently* or *sequentially* integrating SRAM cells and flash EPROM cells onto a single silicon substrate. As discussed above, neither Mehta, Yoo nor their combination teaches or suggests forming a SRAM and an EEPROM on a single substrate using a combination of a LOCOS and STI isolation process. In column 2, lines 18-26, Yoo states the following:

It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining a SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating a SRAM and an EEPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Therefore, it would not have been obvious to one skillful in the art, that Yoo could have been combined with Mehta to disclose the current invention. Further, Yoo appears to be teaching away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate, therefore it would not have been obvious to one skillful in the art from the teachings of Yoo, that a LOCOS and STI isolation process could have been used to form a SRAM and an EEPROM on a common substrate.

The independent Claim 1 is directed to a semiconductor device which comprises a common substrate, a SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM implemented on the common substrate and isolated by a second isolation technique. As described above, neither Mehta, Yoo nor their combination, teach or suggest a SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM implemented on the common substrate and isolated by a second isolation technique. For at least these reasons, the independent Claim 1 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 2, 3, and 4 are dependent on the independent Claim 1. As discussed above, the independent Claim 1 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claims 2, 3, and 4 are allowable as being dependent on an allowable base claim.

The independent Claim 5 is directed to a system for allowing different types of isolation techniques during fabrication of a semiconductor device. The system of Claim 5 comprises a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented

during processing. The system of Claim 5 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device, implemented on the second portion of the substrate. As discussed above, neither Mehta, Yoo nor their combination teach implementing an SRAM device, isolated by a first isolation technique, on a common substrate with a flash EPROM device, isolated by a second isolation technique. For at least these reasons, the independent Claim 5 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 6, 7, and 8 are all dependent on the independent Claim 5. As discussed above, the independent Claim 5 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claims 6, 7 and 8 are also allowable as being dependent on an allowable base claim.

The independent Claim 9 is directed to a semiconductor device comprising a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing. The device of Claim 9 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device implemented on the second portion of the substrate. As discussed above, neither Mehta, Yoo nor their combination teach implementing an SRAM device, isolated by an STI technique, on a common substrate with a flash EPROM device, isolated by a LOCOS isolation technique. For at least these reasons, the independent Claim 9 is allowable over the teachings of Mehta, Yoo and their combination.

Claim 10 is dependent on the independent Claim 9. As discussed above, the independent Claim 9 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claim 10 is also allowable as being dependent on an allowable base claim.

Within the Response to Argument section of the Office Action, it is stated that the discussion on the limitations of a method of making the device is irrelevant in the present application, since the Applicant elected the device claims and withdrew the method claims in the previous amendment. The Applicant respectfully disagrees with this statement.

As discussed above, the pending claims have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoo in view of Mehta. The discussion on the limitations of the LOCOS and STI isolation techniques is relevant since it limits the applicability of the teachings of Yoo in view of Mehta, to the present invention. Within the Office Action, it is indicated that the teachings of Yoo in view of Mehta, disclose a common substrate, a SRAM device implemented on the common substrate and isolated by a first isolation technique, a flash EPROM implemented on the common substrate and isolated by second isolation technique. As discussed above, the teachings of Mehta do not indicate that the first and second isolation technique can be

applied to isolate a SRAM and a EEPROM on a common IC. Moreover, because of the different fabrication processes for a SRAM and an EEPROM, it would have been inherently difficult to fabricate a SRAM and EEPROM on the same IC. Accordingly, the combination of the first and second isolation method disclosed in Mehta could not have been combined with the teachings of Yoo to disclose a common substrate, a SRAM device implemented on the common substrate and isolated by a first isolation technique, a flash EPROM implemented on the common substrate and isolated by the second isolation technique, since the limitations of the LOCOS and STI isolation methods disclosed would render an unreasonable or unexpected expectation of success. Thus, for at least these reasons, the discussion limitations of the LOCOS and STI isolation technique are pertinent to the present application.

For the reasons given above, the Applicant respectfully submits that the claims are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (650) 833-0160 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: November 26, 2001

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CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington D.C. 20231

HAVERSTOCK & OWENS LLP

Date: 11/26/01 By: TW